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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,853	12/08/2003	Ju-Il Lee	51876P414	4256

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,853	LEE, JU-IL	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *1-4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 and 7-13* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/08/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 03/28/05 has been entered.

Election/Restriction

2. Applicant's election without traverse of Group II, claims 5-13, in the Paper filed 03/28/05 is acknowledged.

Oath/Declaration

3. The oath/declaration filed on 12/08/2003 is acceptable.

Drawings

4. The formal drawings filed on 12/08/2003 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statement filed on 12/08/2003 has been considered.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 5,12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of EL GAMAL ET AL. (6,642,543) and HUANG ET AL. (6,146,795).

The admitted prior art discloses a method for manufacturing a CMOS image sensor, comprising the steps of a) preparing a semiconductor substrate 110 incorporating therein a p-type epitaxial layer 112 therein, wherein the semiconductor substrate 110 is divided into two parts of which one part is defined as a pixel array 101 and the other part is defined as a logic circuit 102, the pixel array 101 being isolated from the logic circuit 102 by means of a field oxide region (no part #, see paragraph 0005) therebetween; b) forming a first gate insulator 134 on a top face of the p-type epitaxial layer 112; and c) forming a photodiode (BPD) and a plurality (Tx, Rx, Dx, and Sx) of transistors in the pixel array 101 and at least one transistor 150 in the logic circuit 102 for processing a signal from the pixel array 101. Note figure 1 and paragraphs 0005-0012 of the instant application. The admitted prior art does not disclose the steps of a)

forming the first gate insulator on the top face of the p-type epitaxial layer of SiO_2 by thermally oxidizing the p-type epitaxial layer; b) forming a mask (resist) on a top face of the first gate insulator in the pixel array; c) removing the first gate insulator in the logic circuit by using the mask; d) removing the mask in the pixel array using a thinner; and e) forming a second gate insulator on the top face of the first gate insulator in the pixel array and a top face of the p-type epitaxial layer in the logic circuit.

However, El Gamal et al. discloses a CMOS image sensor with a pixel array 570 having thick (double-gate) gate insulators and a logic circuit 540-550 having thin gate insulators. At column 5 lines 22-25 El Gamal et al. explain that the thicker gate insulators in the pixel array allow the pixels to have higher dynamic range (i.e., the camera containing the pixel array produces brighter brights and darker darks). El Gamal et al. supplies no method whatsoever for producing thicker gate oxides in the pixel array. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. This is not a fatal flaw, enablement-wise, for El Gamal et al.'s patent, however, because prior to El Gamal et al.'s invention Huang et al. disclosed a method of producing thicker and thinner gate oxides comprising a) a step (step 20 in figure 2) of forming an SiO2 first gate insulator on a top face of the p-type epitaxial layer by thermally oxidizing the p-type epitaxial layer; b) a step (step 22 in figure 2) of forming a mask (resist) on a top face of the first gate insulator in the pixel array; c) a step (step 30 in figure 2) of removing the first gate insulator in the logic circuit by using the mask; d) a step

(step 32 in figure 2) of removing the mask in the pixel array using a thinner; and e) a step (step 34 in figure 2) of forming the second gate insulator on the top face of the first gate insulator in the pixel array and a top face of the p-type epitaxial layer in the logic circuit; Note figure 2, column 2 lines 62-67, and column 3 lines 1-9 of Huang et al. Therefore, it would have been obvious to a person having skill in the art to augment the admitted prior art's method for manufacturing a CMOS image sensor with the steps of a) forming an SiO2 first gate insulator on a top face of the p-type epitaxial layer by thermally oxidizing the p-type epitaxial layer; b) forming a mask (resist) on a top face of the first gate insulator in the pixel array; c) removing the first gate insulator in the logic circuit by using the mask; d) removing the mask in the pixel array using a thinner; and e) forming the second gate insulator on the top face of the first gate insulator in the pixel array and a top face of the p-type epitaxial layer in the logic circuit such as suggested by El Gamal et al. and Huang et al. in order to allow the pixels to have higher dynamic range to thus provide a camera containing the pixel array with brighter brights and darker darks.

B. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of EL GAMAL ET AL. (6,642,543) and HUANG ET AL. (6,146,795), as applied to claim 5 above, and further in view of AHN (5,804,491).

The admitted prior art, El Gamal et al., and Huang et al., suggest a method for manufacturing a CMOS image sensor with all the limitations of claims 7-9

except a step of removing a gate insulator by wet-etching with HF or BOE. Note figure 1 and paragraphs 0005-0012 of the instant application. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. Note figure 2, column 2 lines 62-67, and column 3 lines 1-9 of Huang et al.

However, Ahn discloses a method for manufacturing with a step of removing a gate insulator by wet etching with HF or BOE. Note column 5 lines 28-31 of Ahn. Therefore, it would have been obvious to a person having skill in the art to replace the thinner of Huang et al.'s step of removing a gate insulator with the HF or BOE such as taught by Ahn in order to quickly and fully remove the gate insulator to thus provide more efficient manufacture

C. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over THE ADMITTED PRIOR ART in view of EL GAMAL ET AL. (6,642,543) and HUANG ET AL. (6,146,795), as applied to claim 5 above, and further in view of HORI ET AL. (5,707,487).

The admitted prior art, El Gamal et al., and Huang et al., suggest a method for manufacturing a CMOS image sensor with all the limitations of claims 7-9 except a step of removing a mask using sulfuric acid or an O2 plasma etch. Note figure 1 and paragraphs 0005-0012 of the instant application. Note figure 5, column 4 lines 51-58, and column 5 lines 22-25 of El Gamal et al. Note figure 2, column 2 lines 62-67, and column 3 lines 1-9 of Huang et al.

However, Hori et al. discloses a method for manufacturing with a step of removing a mask using sulfuric acid or an O2 plasma etch. Note column 2 lines

38-41 of Hori et al. Therefore, it would have been obvious to a person having skill in the art to replace Huang et al.'s step of removing a mask with the step of removing a mask using sulfuric acid or an O2 plasma etch such as taught by Hori et al. in order to quickly and fully remove the mask to thus provide more efficient manufacture

Allowable Subject Matter

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
08/05